

PATENT APPLICATION

Sheet 1 of 4

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200300182-1

APPLICATION NO.

10698271

CONFIRMATION NO.

APPLICANT

Boon S ong Ang et al.

FILING DATE

GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
DC	1A	6,204,690	Mar. 20, 2001	Young et al.	
DC	1B	6,243,851	Jun. 5, 2001	Hwang et al.	
DC	1C	6,292,022	Sep. 18, 2001	Young et al.	
DC	1D	6,553,395	Apr 22, 2003	Marshall et al.	
DC	1E	6,353,841	Mar. 5, 2003	Marshall et al.	
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

DC	1Q	V. Kathail, et al., PICO (Program In, Chip Out) : Automatically Designing Custom Computers, IEEE Computer, September 2002, 35(9), pp. 39-47.
DC	1R	S. C. Goldstein, et al., PipeRench: A Reconfigurable Architecture and Compiler, IEEE Computer, April 2000, 33(4), pp. 70-77
DC	1S	S. C. Goldstein, et al., PipeRench: A Coprocessor for Streaming Multimedia Acceleration, In Proceedings of the 26th Annual International Symposium on Computer Architecture, 1999, pp. 28-39.

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FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
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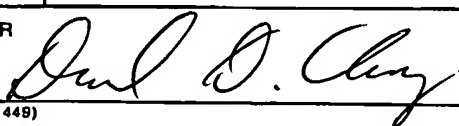
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	2L					
	2M					
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	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

OC	2Q	V. Betz and J. Rose, Effect of the Prefabricated Routing Track Distribution on FPGA Area-Efficiency, IEEE Transactions on VLSI, Sept. 1998, 6(3), pp. 445-456.
OC	2R	Emre Özer, Sanjeev Banerjia, and Thomas M. Conte, Unified Assign and Schedule: A New Approach to Scheduling for Clustered Register File Microarchitectures, In Proceedings of the 31th Annual International Symposium on Microarchitecture (MICRO-31), Dallas, Texas, 1998, pp. 308-315.
OC	2S	M.C. Papaefthymiou, Understanding Retiming Through Maximum Average-Delay Cycles, Mathematical Systems Theory, 1994, 1(27), pp. 65-84.

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<p>FORM PTO-1449</p> <p>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</p> <p align="center">(Use several sheets if necessary)</p>	<p>ATTY. DOCKET NO. 200300182-1</p> <p>APPLICANT Bo n Seong Ang t al.</p> <p>FILING DATE</p>	<p>APPLICATION NO. 10698271</p> <p>GROUP</p>	<p>CONFIRMATION NO.</p>
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3L				
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3P				

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

<i>gc</i>	3Q	J. Babb, R. Tessier, and A. Agarwal, Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators, In Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines, Los Alamitos, CA 1993, pp. 142-151.
<i>gc</i>	3R	J.S. Rose and S. Brown, Flexibility of Interconnection Structures for Field-Programmable Gate Arrays, IEEE JSSC, March 1991, 26(3), pp. 277-282.
<i>gc</i>	3S	S. Note, et al., Cathedral III: Architecture driven high-level synthesis for high throughput DSP applications, In Proceedings of the 28th ACM/IEEE Design Automation Conference, DAC 91, San Francisco, CA, 1991, pp. 597 - 602.

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Paul D. Chy

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

<i>gc</i>	4Q	Constantine N. ANAGNOSTOPOULOS, Paul P. K. LEE, Application-Specific Integrated Circuits, The Electronics Handbook, pp. 731-748, CRC Press, Boca Raton FL, 1996.
<i>gc</i>	4R	Bradley K. FAWCETT, Software Development Tools for Field Programmable Gate Array Devices, The Electronics Handbook, pp. 784-793, CRC Press, Boca Raton FL, 1996.
	4S	

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Paul D. Casey

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2/18/05